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10/730,467	12/08/2003	Steven J. Tu	INTEL/17879	2887

7590 09/26/2005

GROSSMAN & FLIGHT LLC
Suite 4220
20 North Wacker Drive
Chicago, IL 60606-6357

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,467	TU ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-17,19-24 and 26-30* is/are rejected.

7)☒ Claim(s) *5,11,18 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Substitute "124, 134, and 144," by --126, 136, and 146,--in lines 1 and 7 on page 3.

Substitute "126, 136, and 146," by --124, 134, and 144,-- in lines 1, 2, 4, and 5 on page 3.

Substitute "(TPID) 262" by --(TPID) 272--in line 23 on page 8.

Appropriate correction is required.

Claim Objections

2. Claims 2-7, 9-20, 22-27, 29, and 30 are objected to because of the following informalities:

Substitute "A method" by --The method-- in line 1 of the claims 2-7, 29, and 30, respectively.

Substitute "A machine" by --The machine-- in line 1 of the claims 9-14, respectively.

Substitute "An apparatus" by --The apparatus-- in line 1 of the claims 16-20, respectively.

Substitute "A processor" by --The processor-- in line 1 of the claims 22-27, respectively.

The claim 15 recites the subject matter "the interrupt dispatch information" in lines 4-5. However, it has not been specifically clarified in the claim 15. Therefore, the Examiner presumes that the term "the interrupt dispatch information" could be considered as --an interrupt dispatch information-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6, 7, 15-17, 19-24, and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa [US 6,237,058 B1].

Referring to claim 1, Nakagawa discloses a method (i.e., a method for interrupt load distribution; See Abstract) comprising:

- generating an interrupt weighted average (IWA) (i.e., interrupt load distribution schedule) for each of a plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based on interrupt dispatch information (i.e., based on information from processor statistical information table 12 and interrupt schedule information table 12 in Fig. 1) associated with the plurality of processors (See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65) and
- identifying a target processor (i.e., designating a destination processor) from the plurality of processors based on the IWAs (i.e., said interrupt load distribution schedule) to dispatch an interrupt (See col. 7, line 66 through col. 8, line 22).

Referring to claim 2, Nakagawa teaches

- generating the IWA (i.e., interrupt load distribution schedule) for each of the plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based on a processor interrupt loading history level (i.e., CPU activity ratio on the processor statistical information table 12 in Fig. 2; See col. 5, lines 63-67).

Referring to claim 3, Nakagawa teaches

- identifying a weight (i.e., activity ratio) associated with a processor interrupt loading history level (See Fig. 6 and col. 7, lines 12-47).

Referring to claim 4, Nakagawa teaches

- storing a weight (i.e., CPU activity ratio) of one or more interrupt load balancing parameters (i.e., CPU activity ration - system mode, user mode, under use of process executing under a processor bind, number of processes requesting a bind on the processor statistical information table 12 in Fig. 2), and
- calculating the IWA (i.e., interrupt load distribution schedule) for each of the plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based the stored weight (i.e., said CPU activity ratio) of the one or more interrupt load balancing parameters (i.e., based on information from processor statistical information table 12 and interrupt schedule information table 12 in Fig. 1; See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65).

Referring to claim 6, Nakagawa teaches

- identifying the target processor (i.e., designating a destination processor) from the plurality of processors based on the IWAs (i.e., said interrupt load distribution schedule) to dispatch one of a hardware interrupt and a software interrupt (e.g., dispatching reset/dump interrupts and software interrupts; See col. 8, lines 39-44).

Referring to claim 7, Nakagawa teaches

- generating an interrupt message (i.e., interrupt notification) to send to the target processor (i.e., designated processor; See col. 8, lines 35-44).

Referring to claim 15, Nakagawa discloses an apparatus (i.e., an interrupt load distribution system in Fig. 1) comprising:

- an interrupt load balancing policy register (ILBPR) (i.e., interrupt schedule information table 13 of Fig. 1) to store one or more weights corresponding to one or more interrupt load balancing

parameters (i.e., load distribution schedules corresponding to interrupt level, interrupt source, ... in Fig. 3);

- a plurality of target processor control registers (TPCRS) (i.e., processor statistical information table 12 of Fig. 2) to store an interrupt dispatch information (i.e., CPU activity ratio) associated with a plurality of processors (i.e., CPU activity ratios associated with a processor group 50 in Fig. 1);
- a weighted average generator (i.e., interrupt scheduler 20 of Fig. 1; See col. 6, lines 6-21) to generate an interrupt weighted average (IWA) (i.e., interrupt load distribution schedule) for each of the plurality of processors (i.e., processor (1) ... processor (N) in said processor group 50 in Fig. 1) based on the weight (i.e., values of said load distribution schedules) corresponding to the one or more interrupt load balancing parameters (i.e., interrupt level, interrupt source, ... on the interrupt schedule information table 13 in Fig. 3) and the interrupt dispatch information associated with the plurality of processors (i.e., CPU activity ratios associated with said processor group; See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65); and
- a target processor selector (i.e., I/O control part 30 of Fig. 1) to identify a target processor (i.e., destination processor) from the plurality of processors based on the IWAs to dispatch an interrupt (See col. 7, line 66 through col. 8, line 44).

Referring to claim 16, Nakagawa teaches

- the weight (i.e., interrupt load distribution schedule) comprising a processor interrupt loading history weight (i.e., CPU activity ratio on the processor statistical information table 12 in Fig. 2; See col. 5, lines 63-67).

Referring to claim 17, Nakagawa teaches

- the interrupt dispatch information (i.e., CPU activity ratio) comprising a processor interrupt loading history level (i.e., CPU activity ratio on the processor statistical information table 12 in Fig. 2; See Fig. 6 and col. 7, lines 12-47).

Referring to claim 19, Nakagawa teaches

- the target processor selector (i.e., I/O control part 30 of Fig. 1) generates an interrupt message (i.e., interrupt notification) to send to the target processor (i.e., designated processor; See col. 8, lines 35-44).

Referring to claim 20, Nakagawa teaches

- the interrupt comprising one of a hardware interrupt and a software interrupt (e.g., dispatching reset/dump interrupts and software interrupts; See col. 8, lines 39-44).

Referring to claim 21, Nakagawa discloses a processor system (i.e., an interrupt load distribution system in Fig. 1) comprising:

- an input/output controller (i.e., I/O control part 30 of Fig. 1) programmed to request an interrupt (See col. 8, lines 22-44); and
- a multi-processor programmable interrupt controller (MPIC) (i.e., interrupt scheduler 20 of Fig. 1; See col. 6, lines 6-21) programmed
    - to generate an interrupt weighted average (IWA) (i.e., interrupt load distribution schedule) for each of a plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based on interrupt dispatch information (i.e., based on information from processor statistical information table 12 and interrupt schedule

information table 12 in Fig. 1) associated with the plurality of processors (See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65) and

- to identify a target processor (i.e., designating a destination processor) from the plurality of processors based on the IWAs (i.e., said interrupt load distribution schedule) to dispatch the interrupt request (See col. 7, line 66 through col. 8, line 22).

Referring to claim 22, Nakagawa teaches the MPIC (i.e., interrupt scheduler 20 of Fig. 1) is programmed to

- generate the IWA (i.e., interrupt load distribution schedule) for each of the plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based on a processor interrupt loading history level (i.e., CPU activity ratio on the processor statistical information table 12 in Fig. 2; See col. 5, lines 63-67).

Referring to claim 23, Nakagawa teaches the MPIC (i.e., interrupt scheduler 20 of Fig. 1) is programmed

- to store weight (i.e., CPU activity ratio) of the interrupt dispatch information (i.e., information from processor statistical information table 12 and interrupt schedule information table 12 in Fig. 1), and
- to calculate the IWA (i.e., interrupt load distribution schedule) for each of the plurality of processors (i.e., processor (1) ... processor (N) in a processor group 50 in Fig. 1) based the stored weight (i.e., said (i.e., CPU activity ratio) of the interrupt dispatch information (i.e., based on information from processor statistical information table 12 and interrupt schedule information table 12 in Fig. 1; See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65).

Referring to claim 24, Nakagawa teaches the MPIC (i.e., interrupt scheduler 20 of Fig. 1) is programmed to

- identify a weight (i.e., activity ratio) associated with a processor interrupt loading history level (See Fig. 6 and col. 7, lines 12-47).

Referring to claim 26, Nakagawa teaches the MPIC (i.e., interrupt scheduler 20 of Fig. 1) is programmed to

- generate an interrupt message (i.e., interrupt notification) to send to the target processor (i.e., designated processor; See col. 8, lines 35-44).

Referring to claim 27, Nakagawa teaches

- the interrupt comprising one of a hardware interrupt and a software interrupt (e.g., dispatching reset/dump interrupts and software interrupts; See col. 8, lines 39-44).

Referring to claim 28, Nakagawa discloses a method (i.e., a method for interrupt load distribution; See Abstract) comprising:

- determining values (i.e., CPU activity ratios) for a plurality of interrupt load balancing parameters (i.e., CPU activity ration - system mode, user mode, under use of process executing under a processor bind, number of processes requesting a bind on the processor statistical information table 12 in Fig. 2) for each of a plurality of processors (i.e., processor (1) ... processor (N) in said processor group 50 in Fig. 1; See Figs. 5 and 6, and col. 6, line 62 through col. 7, line 65);
- applying a load balancing policy (See col. 5, lines 30-33 and Fig. 6) to the values (i.e., said CPU activity ratios) for the plurality of interrupt load balancing parameters to form a plurality of

values (i.e., values on the interrupt schedule information table 13 of Fig. 3) indicative of an interrupt-related performance of each of the plurality of processors (See col. 6, lines 39-45); and

- identifying one of the plurality of processors as a target processor (i.e., designating destination processor) to receive an interrupt based on the values indicative of the interrupt-related performance (i.e., load distribution schedules corresponding to interrupt level, interrupt source, ... in Fig. 3) of each of the plurality of processors (See col. 7, line 66 through col. 8, line 44).

Referring to claim 29, Nakagawa teaches

- determining values for a processor interrupt loading history parameter (i.e., CPU activity ratio on the processor statistical information table 12 in Fig. 2; See col. 5, lines 63-67).

Referring to claim 30, Nakagawa teaches

- applying an interrupt weighted average (i.e., interrupt load distribution schedule) to each of the values (i.e., activity ratio) for a processor interrupt loading history parameter (See Fig. 6 and col. 7, lines 12-47).

5. Claims 8-10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa [US 6,237,058 B1] in view of what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo].

Referring to claim 8, all of the claim limitations have already been discussed/addressed with respect to claim 1; with the exception of machine readable medium storing instructions, which when executed, cause a machine to perform operations (e.g., memory having a computer software program).

The Examiner takes Official Notice that said method in the claim 1 being implemented in machine executable code for instructing a machine (i.e., a computer software program), and being stored in a

machine readable medium (i.e., memory), is well known to one of ordinary skill in the art, as evidenced by Luo (See Claim 9, lines 2-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said method of the claim 1 in said machine executable code for instructing a machine (i.e., a computer software program), and being stored in said machine readable medium (i.e., memory) since it would have provided a better flexibility of implementing said method than a hardware implementation, such as an easy modification, etc.

Referring to claims 9, 10, 12, and 13, all of the claim limitations in each of the claims 9, 10, 12, and 13 have already been discussed/addressed with respect to each of the claims 2, 3, 5, and 7, respectively.

Referring to claim 14, Luo teaches the machine readable medium (i.e., memory) comprising random access memory (i.e., RAM; See col. 6, lines 50-56).

Allowable Subject Matter

6. Claims 5, 11, 18, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and further rewritten or amended to overcome the claim objections under minor informality, set forth in this Office action, respectively.

7. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 5, 11, 18, and 25, the claim limitations are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest identifying a target processor associated with the highest IWA from the plurality of processors.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rankin et al. [US 6,813,665 B2] disclose interrupt method, system and medium.

Pawlowski et al. [US 6,219,741 B1] disclose transaction supporting interrupt designation redirection and level triggered interrupt semantics.

Arndt et al. [US 6,189,065 B1] disclose method and apparatus for interrupt load balancing for PowerPC processors.

Gronemeyer [US 5,382,950 A] discloses device for implementing an interrupt distribution in a multi-computer system.

Kim et al. [US 2003/0105798 A1] disclose method and apparatus for distributing interrupts.

Kennedy et al. [US 5,446,910 A] disclose interrupt controller with automatic distribution of interrupts for a multiple processor computer system.

Jahnke [US 2003/0120702 A1] discloses load balanced interrupt handling in an embedded symmetric multiprocessor system.

Oner [US 2005/0078694 A1] discloses packet manager interrupt mapper.

Masanori [JP 08-329022] discloses input/output process load decentralization control system for multiprocessor system.

The Examiner refers to Masanori [JP 08-329022] reference as a prior art made of record and not relied upon the claim rejection(s) in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicants. However, the Examiner cautions the Applicants that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the

original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/